Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 1-3. These sheets replace the original sheets.

Attachments

Remarks/Arguments:

Applicants' disclosure is directed to a gate driver for forcing a power transistor having a gate electrode to either conduct or shut off. The gate driver includes a first current source and a second current source. The first current source outputs a first current that lowers the electric potential of the gate electrode and causes the power transistor to begin conducting The second current source outputs a second current that raises the electric potential of the gate electrode and causes the power transistor to shut off. Current-source control information determines the value of the first current and the second current respectively. Accordingly, the first current controls the time it takes to fully shut off the power transistor and the second current controls the time it takes to cause the power transistor to begin fully conducting.

Claims 1, 3 and 5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kogushi (U.S. Patent Number 6,236,239 B1). Further, claims 1, 3 and 5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chen (U.S. Patent Number 5,081,380). It is respectfully submitted, however, that the claims are patentable over the art of record for the reasons set forth below.

Kogushi, as shown in Fig. 1, is directed to an output-buffer circuit. The circuit includes a current source 4/5, a current source 6/7 and a bias circuit 21. Output VP/VN of bias circuit 21 controls the value of the current output from current sources 4/5 and 6/7 respectively.

Chen, as shown in Fig. 1, is directed to a time delay circuit. The time delay circuit includes a current source M1/M2, a current source M4/M3 and a reference current source 12. Reference current source 12 controls the respective values of both IREF1 of current source M1/M2 and IREF2 of current source M4/M3. Current values IREF1 and IREF2 charge or discharge a capacitive load 5 in order to control time delay of a signal.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> A gate driver for forcing a power transistor including a gate electrode insulated with oxide film into conduction or shut-off...
>
> ...a first time period from the shut-off state to the conductive state of the power transistor is controlled with the first current value....

....a second time period from the conductive state to the shut-off state of the power transistor is controlled with the second current value....

This means that both the time it takes to cause the power transistor to fully conduct and the time it takes the power transistor to fully shut off are controllable. The first current value controls the time it takes to cause the power transistor to fully conduct. Similarly, the second current value controls the time it takes to cause the power transistor to fully shut off. This feature is found in the originally filed application at page 12, line 2 through page 13, line 6. No new matter has been added.

Kogushi discloses controlling the time it takes to cause transistors 11 and 13 to fully conduct. However, Kogushi's transistors 11 and 13 are instantly shut off. That is, the time it takes transistors 11 and 13 to fully shut off is not controllable. Therefore, Kogushi discloses time control only in causing the transistors to fully conduct but not in causing the transistors to fully shut off. In other words, current source 4/5 controls the time it takes to change transistor 11 from shut-off state to conductive state, but transistor 13 instantly shuts off transistor 11. Similarly, current source 6/7 controls the time it takes to change transistor 10 from shut-off state to conductive state, but transistor 12 instantly shuts off transistor 10.

This is different because Applicants' power transistor is fully controllable both in the time it takes to cause the power transistor to fully conduct and in the time it takes to cause the power transistor to fully shut off. By contrast, Kogushi's transistor is only controllable in the time it takes to cause the transistors to fully conduct. The time it takes to fully shut down Kogushi's transistors is not controllable.

Chen discloses controlling the time it takes to charge or discharge a capacitive load M5 in order to produce a time-delayed signal at node 110. The time delay signal is output (VOUT) by means of inverters 24 and 25 of CMOS construction driven by a 5V power source VDD. (See column 3, lines 57-58). Consequently, Chen discloses a time-delay circuit for small signal processing, but does not disclose any gate driver for driving a power transistor. In other words, charging or discharging the capacitive load 5 does not cause a gate driver to conduct or shut off.

This is different because Applicants' first and second currents control the time it takes to cause a power transistor to fully conduct or fully shut off. By contrast, Chen's currents control the time it takes to charge or discharge a capacitive load. Neither Chen's capacitive load nor Chen's currents cause a power transistor to conduct or shut off. In this way, Chen does not disclose, as Applicant does, a gate driver for driving a power transistor.

It is because Applicants' include the feature of a gate driver for forcing a power transistor including a gate electrode insulated with oxide film into conduction or shut-off...the time of change from the shut-off state to the conductive state of the power transistor is controlled with the first current value...the time of change from the conductive state to the shut-off state of the power transistor is controlled with the second current value, that the following advantages are achieved. Applicants' gate controller reduces switching noises caused by a sharp transition in the transistor from fully conducting to fully shut off, and vice versa. Further, it reduces malfunctions in peripheral devices or circuits caused by such a sharp transition. Finally, Applicants' gate driver can be used to drive peripheral devices such as, for example, a motor.

Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 3-6 include all the features of claim 1 from which they depend. Thus, claims 3-6 are also patentable over the art of record for the reasons set forth above.

Claims 1-6 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. These claims have been amended to remove any alleged indefiniteness, thus obviating the rejection. All claims as presently amended are fully compliant with 35 U.S.C. § 112. Withdrawal of this rejection is respectfully requested.

Claim 2 was indicated as being allowable if amended to overcome the rejections under 35 U.S.C. § 112. The required changes have been made.

The drawings were amended in accordance with Examiner's recommendations.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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LEA/bj

Attachments: Figures 1, 2, and 3 (2 sheets)

Dated: December 14, 2006

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The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

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December 14, 2006

Beth Johnson

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